PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Edward Brian Boles et al.**	§	Group Art Unit: **2186**
Serial No.: **10/796,771**	§	Examiner: **THOMAS, SHANE M.**
Filed: **03/09/2004**	§	
Title: **"MICROCONTROLLER INSTRUCTION SET"**	§	Atty. Docket No.: **068354.1410**

MAIL STOP AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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MPEP 503

I HEREBY CERTIFY THAT I HAVE A REASONABLE BASIS FOR BELIEF THAT THIS CORRESPONDENCE IS BEING SUBMITTED TO THE UNITED STATES PATENT AND TRADEMARK OFFICE VIA EFS (ELECTRONICALLY) ON THE DATE INDICATED BELOW, AND IS ADDRESSED TO:
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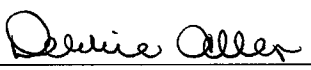

DEBBIE ALLEN, NOVEMBER 30, 2006

DATE OF SUBMISSION: NOVEMBER 30, 2006
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RESPONSE UNDER 37 C.F.R. §1.111 TO NON-FINAL OFFICE ACTION, MAILED SEPTEMBER 29, 2006

Dear Sir:

This is a Response to the Non-Final Office Action, mailed September 29, 2006. Applicants respectfully submit the following remarks and amendments set forth below and request favorable action thereon. The amendments are formatted and presented in accordance with the Revised Format for Amendments promulgated earlier in 2003 by the U.S. Patent and

Trademark Office. The three-month shortened statutory period for reply is due December 29, 2006, therefore, Applicants respectfully request that this Response be considered timely filed.

AMENDMENTS

In the Specification

At page 1, lines 4-6, 8, , 9, 12, 14, 17, 19 and 21, please amend paragraph [0001] as indicated:

[0001] This application is a continuation-in-part of U.S. ~~**Serial Number 09/280,112 that was filed on March 26, 1999**~~ **Patent No. 6,708,268** by the same title and to the same inventors as the present application. This application is related to the following applications: U.S. Patent **[[Nos.]]** **No.** 6,055,211 for "FORCE PAGE ZERO PAGING SCHEME FOR MICROCONTROLLERS USING DATA ACCESS MEMORY" by Randy L. Yach, et al.; **U.S. Patent No.** 5,905,880 for "ROBUST MULTIPLE WORK INSTRUCTION AND METHOD THEREFOR" by Rodney J. Drake, et al.; **U.S. Patent No.** 6,192,463 for "PROCESSOR ARCHITECTURE SCHEME WHICH USES VIRTUAL ADDRESS REGISTERS TO IMPLEMENT DIFFERENT ADDRESSING MODES AND METHOD THEREFOR" by Sumit Mitra, et al. ; **U.S. Patent No.** 6,243,798 for "COMPUTER SYSTEM FOR ALLOWING A TWO WORD INSTRUCTION TO BE EXECUTED IN THE SAME NUMBER OF CYCLES AS A SINGLE WORD JUMP INSTRUCTION" by Rodney J. Drake, et al. ; **U.S. Patent No.** 6,029,241 entitled "PROCESSOR ARCHITECTURE SCHEME HAVING MULTIPLE BANK ADDRESS OVERRIDE SOURCES FOR SUPPLYING ADDRESS VALUES AND METHOD THEREFORE" by Igor Wojewoda, Sumit Mitra, and Rodney J. Drake; **U.S. Patent No.** 6,098,160 for "DATA POINTER FOR OUTPUTTING INDIRECT ADDRESSING MODE ADDRESSES WITHIN A SINGLE CYCLE AND METHOD THEREFOR" by Rodney J.